WHAT IS CLAIMED IS

1. A nonvolatile semiconductor memory device, comprising:

a plurality of blocks each having a memory cell array;

a reference cell;

a signal line that supplies a reference signal read from said reference cell to each of said plurality of blocks;

a reference load circuit which is provided in each of said plurality of blocks, and imposes a load on the reference signal that is identical to a load imposed on data that is read from said memory cell array; and

a sensing circuit which is provided in each of said plurality of blocks, and compares the data with the reference signal having the load imposed thereon by said reference load circuit so as to sense the data.

2. The nonvolatile semiconductor memory device as claimed in claim 1, wherein said reference load circuit includes a pass gate that allows the reference signal to go therethrough only in one of the blocks that is selected.

3. The nonvolatile semiconductor memory

device as claimed in claim 2, further comprising a Y gate which is provided in each of said plurality of blocks, and selects the data read from said memory cell array, wherein a gate at a last stage of said Y gate and said pass gate are structurally identical as circuit elements, and are driven by the same potential.

4. The nonvolatile semiconductor memory device as claimed in claim 3, further comprising a gate that allows the reference signal to go therethrough, and corresponds to a gate other than that of the last stage of said Y gate, said gate being provided in common for each of said plurality of blocks and provided in the vicinity of said reference cell.

5. The nonvolatile semiconductor memory device as claimed in claim 3, further comprising:

a boosting circuit which generates a boosted potential that drives the gate at the last stage of said Y gate and said pass gate;

a power supply line which supplies the boosted potential generated by said boosting circuit to each of said plurality of blocks; and

a switch circuit which is provided in each of said plurality of blocks, and supplies the boosted potential to the gate at the last stage of said Y gate and said pass gate only in said one of the blocks that is selected.

6. The nonvolatile semiconductor memory device as claimed in claim 1, wherein said sensing circuit includes a first current-to-voltage conversion circuit which converts a current to a voltage with respect to the data, and said reference load circuit includes a second current-to-voltage conversion circuit which converts a current to a voltage with respect to the reference signal, wherein said first current-to-voltage conversion circuit and said second current-to-voltage conversion circuit have an identical circuit structure.

7. The nonvolatile semiconductor memory device as claimed in claim 1, wherein said sensing circuit includes a first grounding circuit which couples a source potential with respect to the data to a ground, and said reference load circuit includes a second grounding circuit which couples a source potential with respect to the reference signal to the ground, wherein said first grounding circuit and said second grounding circuit have an identical circuit structure.

8. The nonvolatile semiconductor memory device as claimed in claim 7, wherein said sensing circuit further includes a circuit which short-circuits the source potential with respect to the

data to the source potential with respect to the reference signal.

9. The nonvolatile semiconductor memory device as claimed in claim 1, wherein said sensing circuit includes a first precharge circuit which precharges a potential of a bit line adjacent to a drain bit line with respect to the data, and said reference load circuit includes a second precharge circuit which precharges a potential of a bit line adjacent to a drain bit line with respect to the reference signal, wherein said first precharge circuit and said second precharge circuit have an identical circuit structure.

10. The nonvolatile semiconductor memory device as claimed in claim 9, wherein said sensing circuit further includes a circuit which short-circuits the potential of the bit line adjacent to the drain bit line with respect to the data to the potential of the bit line adjacent to the drain bit line with respect to the reference signal.